

IN THE CLAIMS:

A full listing of the claims, including any amendments made by this paper, is provided below:

1-27 (Canceled).

28. (Currently Amended) A microstructure system including:

a wafer portion including a microstructure formed therein, located thereon or supported thereby wherein said wafer portion includes an upper wafer portion and a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, and wherein said microstructure is formed in or located on said upper wafer portion, and wherein said upper wafer portion defines a coverage area in top view; ~~and~~

a plurality of a solderable surface surfaces configured to receive an electronic component thereon in a direct attachment manner, said solderable surface being formed on, located on, or supported by said wafer portion, said solderable surface being electrically or operatively coupled to said microstructure such that an electronic component coupled to solderable surface can control, operate or receive inputs from at least part of said microstructure and wherein said solderable ~~surface is~~ surfaces are formed or located on said lower wafer portion and ~~is are~~ not located within said coverage area such that said solderable ~~surface is~~ surfaces are not positioned under said upper wafer portion and ~~is are~~ exposed to provide ease of access to said solderable ~~surface surfaces, said solderable surfaces being arranged in a pattern; and~~

an electronic component having a plurality of contacts located thereon, said plurality of contacts being arranged in a pattern corresponding to said pattern of said solderable surfaces such that said electronic component is directly mechanically and electrically attachable to said solderable surfaces by a flip chip bonding process and without the use of wire bonds such that said electronic component can control, operate or receive inputs from at least part of said microstructure.

29. (Canceled)

30. (Canceled)

31. (Previously Presented) The microstructure system of claim 28 wherein said upper wafer portion includes an outer perimeter, and wherein said outer perimeter defines said coverage area.

32. (Previously Presented) The microstructure system of claim 28 wherein said lower wafer portion has a coverage area in top view and wherein said coverage area of said upper wafer portion is entirely contained within said coverage area of said lower wafer portion.

33. (Currently Amended) The microstructure system of claim 28 wherein said upper and lower wafer portions are directly coupled together.

34. (Original) The microstructure system of claim 33 wherein said upper wafer and lower wafer portions are coupled together by a photopatternable adhesive.

35. (Original) The microstructure system of claim 34 wherein said photopatternable adhesive is benzocyclobutene.

36. (Previously Presented) The microstructure system of claim 33 wherein said upper wafer and lower wafer portions are coupled together by a relatively low reflow temperature adhesive, said adhesive having a reflow temperature of less than about 125° C.

37. (Currently Amended) The microstructure system of claim 28 wherein said solderable ~~surface is~~ surfaces are a flip chip connection site configured to receive a chip thereon

by flip chip bonding.

38. (Currently Amended) The microstructure system of claim 28 wherein ~~said each~~ solderable surface includes a ~~plurality of~~ conductive ~~pads~~ pad, each pad being electrically isolated from any adjacent pad and having a melting point of less than about 250°C.

39. (Canceled)

40. (Currently Amended) The microstructure system of claim ~~39~~ 28 wherein said electronic component is a chip and wherein said chip is coupled to said solderable ~~surface~~ surfaces by flip chip bonding.

41. (Canceled)

42. (Currently Amended) The microstructure system of claim ~~28~~ 41 ~~further comprising a plurality of electronic components, each electronic component being coupled to one of said plurality of solderable surface, the system~~ further including an external controller coupled to said electronic ~~components~~ component to control the input to or output from said electronic ~~components~~ component ~~via said solderable surfaces~~ to thereby control or monitor the input to or output from said microstructure.

43. (Original) The microstructure system of claim 28 wherein said microstructure is at least one of a sensor or an actuator.

44. (Original) The microstructure system of claim 28 wherein said microstructure is a mirror array including a plurality of movable reflective surfaces.

45. (Currently Amended) The microstructure system of claim 44 further including at

least one component which can control the movement of at least one of said reflective surfaces, wherein said solderable ~~surface is~~ surfaces are electrically or operatively coupled to said at least one component.

46. (Previously Presented) The microstructure system of claim 45 wherein said component is an electrode for controlling the movement of said at least one movable reflective surface when a voltage or current is applied across said electrode.

47. (Previously Presented) The microstructure system of claim 46 wherein at least two electrodes are located below each of said reflective surfaces such that a voltage can be applied across said electrodes to cause the associated reflective surface to move in at least two generally opposite directions.

48. (Original) The microstructure system of claim 44 wherein each reflective surface is individually movable relative to any adjacent reflective surfaces and is individually controllable.

49. (Currently Amended) The microstructure system claim 44 wherein said solderable ~~surface~~ surfaces can carry a sufficient bandwidth to allow an external controller coupled to said solderable ~~surface~~ surfaces and to said electronic component to cause and control the individual movement of each reflective surface relative to any adjacent reflective surfaces.

50. (Previously Presented) The microstructure system of claim 28 wherein said coverage area of said upper wafer portion is smaller than the coverage area of said lower wafer portion.

51. (Previously Presented) The microstructure system of claim 44 wherein said upper wafer portion includes a silicon layer, and wherein said reflective surfaces are non-silicon material located on said silicon layer.

52. (Previously Presented) The microstructure system of claim 44 wherein said upper wafer portion includes a base portion and a plurality of movable portions rotatably coupled to base portion, and wherein each reflective surface is located on one of said movable portions.

53. (Previously Presented) The microstructure system of claim 28 wherein said upper wafer portion includes at least a portion of at least one silicon-on-insulator wafer.

54. (Previously Presented) The microstructure system of claim 28 wherein said lower wafer portion is or includes at least part of a semiconductor wafer, or a ceramic substrate, or a glass substrate, or a printed circuit board.

55 (Previously Presented) The microstructure system of claim 28 wherein said lower wafer portion includes an upper surface facing said upper wafer portion, and wherein said solderable surface is located on said upper surface.

56. (Currently Amended) A microstructure system including:

a lower wafer or wafer portion;

an upper wafer or wafer portion including a microstructure formed therein, located thereon or supported thereby, said upper wafer or wafer portion being positioned generally above said lower wafer or wafer portion and defining a coverage area in top view, wherein said upper wafer or wafer portion is directly coupled to said lower wafer or wafer portion; and

~~a lower wafer or wafer portion located generally below and coupled to said upper wafer or wafer portion~~

~~said lower wafer or wafer portion including an electronic component located thereon or supported thereby~~ directly coupled to said lower wafer or wafer portion and laterally offset from said upper wafer or wafer portion, said electronic component being electrically or operatively coupled to said microstructure such that said electronic component can control,

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operate or receive inputs from at least part of said microstructure, wherein said electronic component is generally not located within said coverage area of said upper wafer or wafer portion such that said electronic component is generally not positioned under said upper wafer or wafer portion and is exposed to provide ease of mounting to said electronic component.

57-112. (Canceled)

113. (Previously Presented) The microstructure system of claim 28 wherein said upper wafer portion and said lower wafer portion are coupled together by an electrically insulating material such that said upper and lower wafer portions are not directly electrically connected.

114. (Currently Amended) The microstructure system of claim ~~39~~ 28 wherein said electronic component is not located within said coverage area such that said electronic component is not positioned under said upper wafer portion to provide ease of mounting said electronic component.

115. (Canceled)

116. (Previously Presented) The microstructure system of claim 28 wherein the entirety of said solderable surface is not located within said coverage area and is not positioned under said upper wafer.

117. (Previously Presented) The microstructure system of claim 56 wherein said lower wafer or wafer portion includes an upper surface facing said upper wafer or wafer portion, and wherein said solderable surface is located on said upper surface.

118. (Currently Amended) A microstructure system including:
an upper wafer portion including a microstructure formed therein, located thereon

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or supported thereby, said upper wafer portion defining a coverage area in top view;

a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, said lower wafer portion including at least one electrode for controlling the movement of at least part of said microstructure;

a solderable surface formed or located on said lower wafer portion, wherein said solderable surface is not located within said coverage area such that said solderable surface is not positioned under said upper wafer portion to provide ease of access to said solderable surface; and

an electronic component coupled to said solderable surface by flip chip bonding without wire bonds and being electrically or operatively coupled to said electrode such that said electronic component can control or operate said electrode to thereby control or operate said microstructure.

119. (Previously Presented) The microstructure system of claim 118 wherein said upper wafer portion and said lower wafer portion are coupled together by an electrically insulating material such that said upper and lower wafer portions are not directly electrically connected.

120. (Previously Presented) The microstructure system of claim 118 wherein said lower wafer portion includes an upper surface facing said upper wafer portion, and wherein said solderable surface is located on said upper surface.

121. (Previously Presented) The microstructure of claim 118 wherein said electronic component is positioned between said lower wafer portion and said upper wafer portion.

122 - 127. (Canceled)

128. (Previously Presented) The microstructure system of claim 118 wherein said electronic component is a separate component that is spaced apart from said electrode.

129. (Currently Amended) A microstructure system including:

a wafer portion including a microstructure formed therein, located thereon or supported thereby wherein said wafer portion includes an upper wafer portion and a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, and wherein said microstructure is formed in or located on said upper wafer portion, and wherein said upper wafer portion defines a coverage area in top view and an exposed area that is outside said coverage area; and

a solderable surface configured to receive an electronic component thereon in a ~~direct attachment manner~~ flip chip attachment process and without wire bonds, said solderable surface being formed on, located on, or supported by said wafer portion, said solderable surface being electrically or operatively coupled to said microstructure such that an electronic component coupled to solderable surface can control, operate or receive inputs from at least part of said microstructure and wherein said solderable surface is formed or located on said lower wafer portion and is ~~not~~ located within said ~~coverage~~ exposed area, wherein said upper wafer portion and said lower wafer portion are coupled together by an electrically insulating material such that said upper and lower wafer portions are not directly electrically connected.

130. (Previously Presented) The system of claim 129 wherein said upper wafer portion and said lower wafer portion are generally electrically insulated such that a current cannot be directly passed between said upper and lower wafer portions.

131. (New) The system of claim 28 wherein said wafer portion includes an exposed area that is outside said coverage area, and wherein electronic component is located generally entirely in said exposed area.

132. (New) The system of claim 28 wherein said upper wafer portion is directly coupled to said lower wafer portion, and said electronics component is directly coupled to said lower wafer portion.

133. (New) The system of claim 28 wherein said microstructure does not include any active electronics positioned directly below said upper wafer portion that can control, operate, or receive inputs from said microstructure.

134. (New) The system of claim 28 wherein said upper wafer portion is directly coupled to said lower wafer portion, and said electronic component is directly attached to said lower wafer portion, and wherein said electronic component is generally not positioned directly under said upper wafer portion.

135. (New) The microstructure of claim 56 wherein said lower wafer or wafer portion includes an exposed area positioned outside of said coverage area of said upper wafer or wafer portion, and wherein the microstructure includes a plurality of solderable surfaces generally located within exposed area of said upper wafer in top view such that said solderable surfaces are not positioned under said upper wafer portion, said solderable surfaces being arranged in a pattern, wherein said electronic component includes a plurality of contacts located thereon, said plurality of contacts being arranged in a pattern corresponding to said pattern of said solderable surfaces such that said electronic component is directly mechanically and electrically attached to said solderable surfaces by a flip chip bonding process and without the use of wire bonds such that said electronic component can control, operate or receive inputs from at least part of said microstructure by the transmission of electrical signals from the electronic component to the lower wafer or wafer portion via the flip chip connections.

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136. (New) The microstructure of claim 56 wherein said electronic component is indirectly electrically or operatively coupled to said microstructure via said lower wafer or wafer portion.

137. (New) The microstructure system of claim 129 wherein said solderable surface includes a plurality of conductive pads arranged in a pattern configured to match a pattern of conductive contacts of an electronic component.